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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,203	09/24/2003	Jeffrey L. Wise	IS01389MCG	6948

23330 7590 01/08/2008
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EXAMINER

PASIA, REDENTOR M

ART UNIT	PAPER NUMBER
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2616

MAIL DATE	DELIVERY MODE
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01/08/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/671,203	Applicant(s) WISE ET AL.	
	Examiner Redentor M. Pasia	Art Unit 2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on October 17, 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 7-12, 14-20 and 22-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-12, 14-20 and 22-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

Applicant's amendment filed on October 17, 2007 has been entered. Claims 1, 2, 5, 9, 12, 16 have been amended. Claims 6, 13, 21 have been canceled. No claims have been added. Claims 1-5, 7-12, 14-20 and 22-23 are still pending in this application, with claims 1, 9, and 16 being independent.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-8 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 5-8 of copending Application No. 10/671/204. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

As to claim 1 of the application, claim 1 of the co-pending application shows a method, comprising: a link receiver providing a plurality of data credits to a link transmitter (claim 1); the link transmitter transmitting a plurality of packets to the link receiver on an ingress link (claim 1), wherein the ingress link has a forward link and a

reverse link (this claim limitation is not explicitly shown, but it would have been obvious to one of ordinary skill in the art that the ingress link has a forward and reverse link), and wherein the plurality of packets are transmitted on the forward link (claim 1); the link receiver storing the plurality of packets in a plurality of receiver buffers (claim 1); the link receiver updating a free buffer pool (claim 1); and the link receiver transmitting a flow control packet to the link transmitter on the reverse link if the free buffer pool contains additional data credits and the reverse link is idle (this claim limitation is not explicitly shown, but it would have been obvious to one of ordinary skill in the art that when the link receiver sends a control packet, it notifies the link transmitter of additional data credits), wherein the flow control packet comprises the additional data credits (claim 1).

As to claim 2 of the application, claim 1 of the co-pending application shows a step of placing the plurality of receive buffer into a free buffer pool as the packet is transmitted out of the plurality of receive buffers.

As to claim 3 of the application, claim 1 of the co-pending application shows that the link receiver transmits a flow control packet to the link transmitter wherein the flow control packets corresponds to additional data credits (additional space in buffer).

As to claim 4 of the application, claim 1 of the co-pending application shows a step of placing the plurality of receive buffers into a free buffer pool as the packet is

transmitting out of the plurality of receiver buffers, wherein the free buffer pool corresponds to additional credits (space).

As to claim 5 of the application, refer to claim 5 of the co-pending application.

As to claim 6 of the application, refer to claim 6 of the co-pending application.

As to claim 7 of the application, refer to claim 7 of the co-pending application.

As to claim 8 of the application, refer to claim 8 of the co-pending application.

Claims 9-12, 14-23 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 17, 19, 21-26 of copending Application No. 10/671,204 (hereinafter 204) in view of copending Application No. 10/671,128 (hereinafter 128).

As to claim 9 of the application, claim 17 of 204, shows a switch, comprising: a plurality of receiver buffers coupled to receive a packet from a link transmitter on an ingress link having a forward link and a reverse link, wherein the packet is stored in the plurality of receiver buffers (claim 17; however claim 17 does not explicitly show a forward link and a reverse link but it is obvious to one of ordinary skill in the art that an ingress link has a forward link and a reverse link); a free buffer pool (claim 17) ; and a

link receiver flow control algorithm (claim 17), However, 204 does not show a step of the link receiver flow control algorithm transmits a flow control packet to the link transmitter on the reverse link if the free buffer pool contains additional data credits and the reverse link is idle, wherein the flow control packet comprises the additional data credits.

Claim 13 (dependent on claim 10) of 128 shows transmitting a flow control packet comprises notifying the link transmitter of an empty portion of a plurality of receiver buffers. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify 204 by having the flow control packet of 128 in order to have an indication whether space is available for transmission of packets from transmitter to sender.

As to claim 10 of the application, refer to claim 9 rejection above.

As to claim 11 of the application, refer to claim 19 of 204, (in view of 128).

As to claim 12 of the application, 204 shows all of the elements except the link transmitter has a plurality of logical channels, and wherein the link transmitter selects to which of the plurality of logical channels to allocate the additional data credits.

128 shows in claim 10, that the link transmitter has a plurality of logical channels, and wherein the link transmitter selects to which of the plurality of logical channels to allocate the additional data credits. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify 204 by having logical channels of 128 in

order to have multiple paths of transmission of control packets from sender to transmitter.

As to claim 14 of the application, refer to claim 21 of 204 (in view of 128).

As to claim 15 of the application, refer to claim 22 of 204 (in view of 128).

As to claim 16 of the application, claim 23 of 204 shows a computer-readable medium containing computer instructions for instructing a processor to perform a method of updating a link transmitter (claim 23), the instructions comprising: a link receiver providing a plurality of data credits to the link transmitter(claim 23); the link transmitter transmitting a plurality of packets to the link receiver on an ingress link (claim 23), wherein the ingress link has a forward link and reverse link (claim 23 does not explicitly show that the ingress link has a forward link and a reverse link but it would have been obvious to one of ordinary skill in the art that an ingress link has a forward link and a reverse link in order to have a path for communications and control communications), and wherein the plurality of packets are transmitted on the forward link (claim 23); the link receiver storing the plurality of packets in a plurality of receiver buffers (claim 23); the link receiver updating a free buffer pool (claim 23). However, 204 does not show the link receiver transmitting a flow control packet to the link transmitter on the reverse link if the free buffer pool contains additional data credits and the reverse link is idle, wherein the flow control packet comprises the additional data credits.

However, 128 shows at claim 19 the link receiver transmitting a flow control packet to the link transmitter on the reverse link if the free buffer pool contains additional data credits and the reverse link is idle, wherein the flow control packet comprises the additional data credits. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify 204 by having the flow control packet of 128 in order to have an indication whether space is available for transmission of packets from transmitter to sender.

As to claim 17 of the application, refer to claim 23 of 204 (in view of 128).

As to claim 18 of the application, 204 shows all of the elements except the flow control packet notifies the link transmitter of an empty portion of the plurality of receiver buffers.

Claim 22 (dependent on claim 19) of 128 shows transmitting a flow control packet comprises notifying the link transmitter of an empty portion of a plurality of receiver buffers. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify 204 by having the flow control packet of 128 in order to have an indication whether space is available for transmission of packets from transmitter to sender.

As to claim 19 of the application, refer to claim 24 of 204 (in view of 128).

As to claim 20 of the application, refer to claim 25 of 204 (in view of 128).

As to claim 21 of the application, refer to claim 26 of 204 (in view of 128).

As to claims 22 and 23, 204 shows all of the elements except the link transmitter and the link receiver operate in a switch fabric network(as to claim 22) and the switch fabric network is one of an Infiniband network and a Serial RapidIO network (as to claim 23).

Claim 25 (dependent on claim 19) of 128 shows the switch fabric network is one of an Infiniband network and a Serial RapidIO network. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify 204 by switch fabric of 128 in order to have a plurality of communications paths on a given physical link.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5, 7-12, 14-20 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bloch et al. (US 6,922,408 B2; hereinafter Bloch) in view of Jones et al. (US 6944173 B1; hereinafter Jones) in further view of Takase et al. (US 7023799 B2; hereinafter Takase)

As to claim 1, Bloch shows a method, comprising: providing from a link a receiver a plurality of data credits to a link transmitter (col. 7, lines 18-21; shows that the receiver updates the available credits and when possible, provides additional credits to the transmitter.); transmitting a plurality of packets from the link transmitter to the link receiver on an ingress link, wherein the ingress link has a forward link and a reverse link, and wherein the plurality of packets are transmitted on the forward link (col. 4, lines 58-63, figure 1; shows switch 20 in a packet switching fabric. The packet switching fabric comprises an Infiniband (IB) fabric. At col. 1, lines 38-40, it shows that the switch port at each end of each physical link includes a transmitter and a receiver for sending packets to and receiving packets from the corresponding port at the other end of the link. At figure 1, link 29 shows an ingress and egress virtual link.); storing the plurality of packets in a receiver buffer at the link receiver (col. 3, lines 27-29; shows a step of receiving the data in the receive buffer responsive to the allocated credits.); updating a free buffer pool at the link receiver (Based from the specification of the application (Wise) at Par. 0033, it shows that free buffer pool represents the empty portion of the receiver buffer. Bloch shows at Figure 5, a flow chart that illustrates a method of reallocation of credits in receive queues 28 after a data packet has passed out of buffer

25. At col. 8, lines 22- 51, shows the different scenarios of credit (of buffer space) reallocation when the packet was passed out of the buffer.); and transmitting a flow control packet from a link receiver to the link transmitter on the reverse link if the free buffer pool contains additional data credits and the reverse link is idle, wherein the flow control packet comprises the additional data credits (col. 1, lines 43-47; show that the transmitter receives a flow control packet from the receiver indicating that additional credit is available. Based from the specification of the application (Wise) at Par. 0049, it shows that if the free buffer pool 330 does contain additional data credits 334 per step 610, then it is determined if reverse link 314 is idle per step 612. Based from this description, the examiner interprets that if there are free space in the buffer, there are additional credits available and this also establishes that the reverse link is idle. This interpretation is applied to the remainder of the office action.). However, Bloch does not show the step of allocating at the link transmitter the plurality of data credits to a plurality of logical channels and Bloch does not show a plurality of receiver buffers.

Jones shows the step of allocating at the link transmitter the plurality of data credits to a plurality of logical channels (Figure 1, plurality of virtual channels, VC0-N; Figure 5; col. 2, lines 13-21). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify method of Bloch to include the selection of logical channels of Jones in order to bypass the need for an acknowledgement packet, resulting in reliable transmissions and efficient use of bandwidth (Jones, col. 2, lines 7-9). Jones does not show a plurality of receiver buffers.

Takase shows a plurality of packet buffers (Figure 2, Packet Buffer 20-1 to 20-n). It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method of modified Bloch to include the plurality of packet buffers of Takase, as shown above, in order to increase the amount of data to be transmitted and/or received in a device.

As to claim 2, further modified Bloch shows the step of updating the free buffer pool at the link receiver comprises the link receiver updating the free buffer pool as one of the plurality of packets is transmitted out of the plurality of receiver buffers (Based from the specification of the application (Wise) at Par. 0033, it shows that free buffer pool represents the empty portion of the receiver buffer. Bloch shows at Figure 5, a flow chart that illustrates a method of reallocation of credits in receive queues 28 after a data packet has passed out of buffer 25. At col. 8, lines 22- 51, shows the different scenarios of credit (of buffer space) reallocation when the packet was passed out of the buffer.).

As to claim 3, further modified Bloch shows that the flow control packet notifies the link transmitter of an empty portion of the plurality of receiver buffers (Bloch: col. 3, lines 63-65; shows that controlling the transmission of the data packets includes sending a flow control packet from the receiving entity to the transmitting entity, informing the transmitting entity of the allocated credits. At col. 4, lines 9-11, shows that

the credits corresponds to space available to the links in a dynamically allocable portion of the receive buffer.).

As to claim 4, further modified Bloch shows that one of the plurality of data credits corresponds to one of the plurality of receiver buffers being empty (Takase: col. 8, lines 34-46, shows that when the level drops largely below the threshold, and after that, packets flow in a rate over the minimum guaranteed bandwidth of 600 Mbps, during a period until the level reaches the threshold TH600, packets are transmitted to the output line at a rate over the minimum guaranteed bandwidth. A level that is largely below the threshold also covers the lowest level possible (an empty buffer).).

As to claim 5, further modified Bloch shows the step of selecting from the plurality of logical channels to allocate the additional data credits at the link transmitter (Jones: Figures 1 and 5; col. 2, lines 13-21).

As to claim 7, further modified Bloch shows that the link transmitter and the link receiver operate in a switch fabric network (Bloch: col. 4, lines 58-63).

As to claim 8, further modified Bloch shows that the switch fabric network is one of an Infiniband network (col. 4, lines 58-63).

As to claim 9, Bloch shows a switch (Figure 1), comprising:
a receiver buffer coupled to receive a packet from a link transmitter on an ingress link having a forward link and a reverse link, wherein the packet is stored in the plurality of receiver buffers (col. 5, lines 7-9; Figure 1; shows Port 24 (receiver) and entity 27 (transmitter) are configured to communicate over a plurality of logical links all of which are carried over physical link 29. At col. 2, lines 15-25, Bloch shows that the receiver has a buffer where it holds data packets that it has receive over the physical link before passing the packets through the switch to another of the ports for further transmission through the fabric and also, that the transmitter transmits packets over a given logical link. Figure 1, link 29 shows an ingress and egress virtual link.); a free buffer pool (col. 6, lines 31-33); a free buffer pool (col. 6, lines 31-33); and a link receiver flow control algorithm, wherein the link receiver flow control algorithm transmits a flow control packet to the link transmitter on the reverse link if the free buffer pool contains additional data credits and the reverse link is idle, wherein the flow control packet comprises the additional data credits (Bloch shows at Figure 5, a flow chart that illustrates a method of reallocation of credits in receive queues 28 after a data packet has passed out of buffer 25. At col. 8, lines 22- 51, shows the different scenarios of credit (of buffer space) reallocation when the packet was passed out of the buffer.). However, Bloch does not show the link transmitter allocates a plurality of data credits to a plurality of logical channels and Bloch does not show a plurality of receiver buffers.

Jones shows that the link transmitter allocates a plurality of data credits to a plurality of logical channels (Figure 1, plurality of virtual channels, VC0-N; Figure 5; col.

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2, lines 13-21). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify method of Bloch to include the selection of logical channels of Jones in order to bypass the need for an acknowledgement packet, resulting in reliable transmissions and efficient use of bandwidth (Jones, col. 2, lines 7-9). Jones does not show a plurality of receiver buffers.

Takase shows a plurality of packet buffers (Figure 2, Packet Buffer 20-1 to 20-n). It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method of modified Bloch to include the plurality of packet buffers of Takase, as shown above, in order to increase the amount of data to be transmitted and/or received in a device.

As to claims 10, 11, 12, 14 and 15, these claims are rejected using the same reasoning set forth in the rejection of claims 3, 4, 5, 7, and 8, respectively.

As to claim 16, this claim is rejected using the same reasoning set forth in the rejection of claim 1. As to the additional claim limitation, a computer-readable medium encoded with computer executable instructions for instructing a processor to perform a method of updating a link transmitter, refer to Bloch, col. 5, lines 2-4.

As to claims 17, 18, 19, 20, 22, and 23, these claims are rejected using the same reasoning set forth in the rejection of claims 2, 3, 4, 5, 7, and 8.

Response to Arguments

Applicant's arguments, see Applicant's Arguments/Remarks pages 7-12, filed October 17, 2007, with respect to the rejection(s) of claim(s) 1-3, 7-10 and 14-23 under Bloch et al. (US 6922408) in view of Florin et al. (US 6594701); Claims 5-6, 12-13 and 20-21 under Bloch et al. (US 6922408) in view of Florin et al. (US 6594701) in further view of Jones et al. (US 6944173) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Bloch et al. (US 6,922,408 B2) in view of Jones et al. (US 6944173 B1) in further view of Takase et al. (US 7023799 B2) for claims 1-5, 7-12, 14-20 and 22-23.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Susnow et al. (US 7,190,667 B2) – note abstract;

Barkey et al. (US 5,825,748) – note abstract;

Bass et al. (US 7,072,299 B2) – note abstract;

Barrack et al. (US 6954424 B2) – note abstract.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

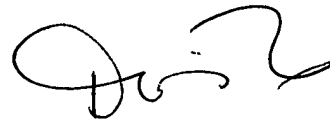
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Redentor M. Pasia whose telephone number is 571-272-9745. The examiner can normally be reached on M-F 7:30am to 4:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris H. To can be reached on (571)272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


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